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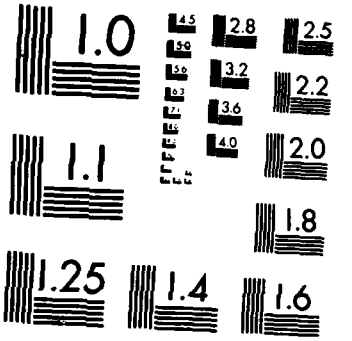

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Gallium Arsenide Integrated Circuits and Technology

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Key efforts in gallium arsenide integrated circuits and technology in the UK and France are reviewed. The review is based on visits to five organizations working in the field, and covers the developments they are pursuing and the potential they exhibit for turning the products of their research into practical processes or manufactured components.

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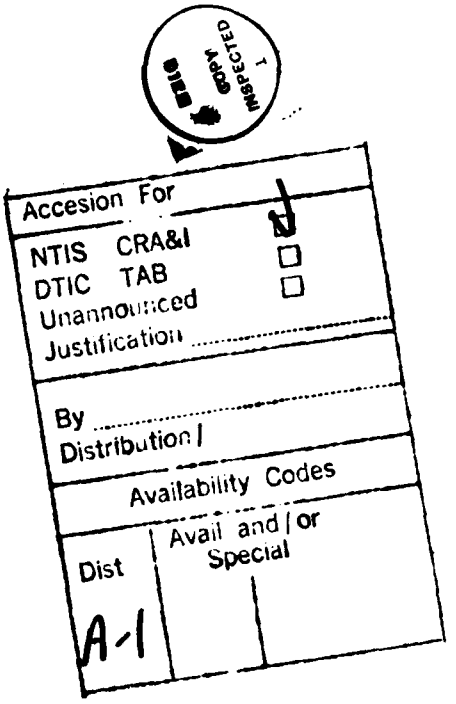

GALLIUM ARSENIDE INTEGRATED CIRCUITS AND TECHNOLOGY

1 INTRODUCTION

This report is a review of some of the key efforts taking place in France and the UK in the area of gallium arsenide (GaAs) integrated circuits (IC's) and technology. It is based on visits to five of the principal companies working in GaAs in the UK and France as well as one MOD-supported research center in the UK. GaAs IC's have performance features that will be of use to "next generation" systems where higher bandwidth or data rate is required. GaAs IC's also offer higher inherent radiation hardness than do silicon IC's, an important feature in many applications.

GaAs IC's are just emerging as a new class of integrated components available for high-speed military systems. Their need and application can be found in any system where an increase in system bandwidth, data rate, or other speed-related parameter is desired. Depending on the type of GaAs IC technology that is used (e.g., enhancement or depletion mode metal Schottky barrier field effect transistors [MESFET's], high-electron mobility transistor [HEMT], heterojunction bipolar transistor [HJBT], etc.), an increase in overall speed or combined speed/power product can be achieved. The increase in performance over similar IC functions fabricated in silicon can be as much as a factor of two to five times. Some will quote even more optimistic performance increases, and these may well be achievable with advanced materials and device structures.

Beyond what is reported in the technical literature and presented at appropriate symposiums, it is important to also look at the production capability of those companies working in the field. While it is necessarily important to pursue advanced materials and structures, the end result should eventually be a component or process that will provide an improvement over existing technology. For an R&D organization to commit to production and manufacturing, many necessary changes in organization, direction, and priorities are required. These are usually best achieved by creating a separate manufacturing organization that is distinct from the R&D unit. A manufacturing IC process has to be frozen to a fixed set of performance parameters with relatively high IC yield being an important goal. The R&D organization should be free to change, modify, and otherwise alter the IC process to suit its goals and direction of experimentation. This same freedom in a manufacturing line will prove to be very hazardous. Once performance parameters are fixed and modeling is put in place for an IC process, designers expect the process on which their design is fabricated to be the same one that their initial models were based on, not an "improved" process that is different.

The six sites chosen for this review were:

- Plessey Research (Caswell), Allen Clark Research Centre, Caswell, Towcester, UK
- GEC, Hirst Research Centre, Wembley, Middlesex, UK
- Royal Signals and Radar Establishment (RSRE), Great Malvern, UK
- STL (Standard Telecommunications Laboratory), GaAs IC Laboratory, Harlow, Essex, UK
- Thomson-CSF, Orsay Cedex, France
- Phillips (LEP), Limiel-Brevannes, France

2 PLESSEY RESEARCH

About 110-120 people are involved with the GaAs effort at Plessey's Research center at Caswell. The main design effort at Plessey concerns monolithic microwave integrated circuits (MMIC's) and other analog RF-based components. Plessey is very involved with both AC and DC modeling of the GaAs devices used for design. Development of an accurate model is one of the most difficult tasks facing any IC design team. Plessey has developed software that takes a DC parameter-based model

and then adds the AC parameters, including the frequency variable MESFET drain conductance, without changing the DC parameters. The primary technology at Plessey Research is a 0.5-micron gate-length MESFET process, with demonstrated capability at 0.25-micron gate-length devices produced with an electron beam (E-beam) direct write-on wafer process (DWW).

Plesey has been fabricating prototype components for their radar division and have successfully designed and built a GaAs IC-based multifunction phased array Radar System. The initial cost of the prototype modules is high, but the design is based on 3-year-old technology and integration levels. Using the currently demonstrated technology, the entire GaAs module could be significantly reduced in size and cost. Replacing the multichip GaAs hybrid circuit with a 3-chip set, and producing modules at realistic production volumes (3000/yr), the cost per module could be reduced by an order of magnitude. Current modules priced at approximately $4500 per unit could be produced for less than $500 per unit.

The GaAs IC R&D effort at Plessey Research consists of about 30 people. The main goals for this unit are:

1. Process characterization.
2. High packing density (HPD) for IC's. A goal of a 1-mm^2 die is driven by the radar effort.
3. A computer-aided design (CAD) system to allow starting with a physical description of a circuit and then extracting all performance and parasitic parameters is being developed.
4. RF on wafer testing for characterization.
5. FET (field effect transistor) amplifiers and frequency doublers. Operation to 20 GHz desired. Class "B" FET amplifiers to improve efficiency of design.
6. Broadband voltage-controlled oscillators (VCO's). 1-chip, 6- to 18-GHz system desired.
7. Yield evaluation for ESA.
8. HJBT process for advanced devices.

To achieve realistic production success, Plessey has created a separate company to produce commercial GaAs components: Plessey III-V. Plessey III-V intends to offer GaAs foundry services as well as producing standard components. The main process pilot line for Plessey III-V is located at Caswell, while the rest of the organization is about 4 miles away. The process currently being used for the production line is based on a 0.9-micron gate length. Having the pilot line at Caswell provides for a good transfer of technology from the research division. The manufacturing pilot line is separate from the R&D process line, and provides the base for a stable manufacturing process. Plessey has already demonstrated very good IC yield for their prototypes, and should continue to develop and provide high-quality components suitable for advanced military applications.

3 GEC--HIRST RESEARCH CENTRE

GEC is also working in the area of GaAs MMIC's. They have produced a variety of prototypes including amplifiers, digital phase shifters with analog control between digital steps, low-noise amplifiers, and traveling wave amplifiers. Their primary technology is based on a 1.0-micron gate-length depletion mode MESFET process. The GEC people use both molecular beam epitaxy (MBE) and ion-implanted material for their MESFETS process. An advanced process based on a 0.5-micron E-beam DWW is also being used for the gate layer with automatic alignment to the ohmic layer. The DWW step is mixed with normal photo steps for the remainder of the fabrication.

Prototype GaAs IC components for a phased array radar have also been produced at GEC and are being assembled into a system by Marconi Instruments. The GaAs components include a switched line phase shifter, an X-Band amplifier, and a mixer. Their demonstrated yield is not as high as desired, and work is

being done on yield enhancement for the process. As yet, GEC has not created a separate division for manufacturing, and the prototypes are being produced on the R&D fabrication line.

A major effort in modeling is being done by Dr. Peter Ladbrooke. He has developed modeling software that can create an electrical model from the physical description of the MESFET or, conversely, the physical properties and description of the MESFET based on the electrical description. This capability allows optimization of the process to produce the desired results. Predicting gate length, recess depth, and implant concentrations based on measured electrical performance is an impressive modeling ability.

4 ROYAL SIGNALS AND RADAR ESTABLISHMENT (RSRE)

RSRE is a MOD-(Ministry of Defence) supported research center of about 2000 people. RSRE maintains close ties with the MOD-funded work that is going on at Plessey, GEC Hirst, and STL, and a good technology exchange seems to be taking place. RSRE is primarily concerned with advanced materials and processes, and does not compete with the efforts being carried out commercially. Once RSRE can demonstrate feasibility of a material or device, the technology is passed on to the commercial sector for development and introductory production.

RSRE has four departments in the device physics area of applied physics; they are: Solid State Physics, Microwave Devices, Microwave Techniques, and Electronic Materials. My visit included an overview of three of these departments.

The Microwave Devices Department includes work in five areas:

- GaAs processing
- New process research
- CAD
- Thin film hybrids
- Fast optical devices

The department's optoelectronics effort consists of about 10 people. They are involved with research involving advanced III-V technology. They consider MOCVD (metallo-organic chemical vapor deposition) as the dominant process for layered GaAs and will try to push the MOCVD process into production. They have demonstrated very high-speed micro-optical modulators based on GaAlAs-GaAs-GaAlAs layered structures. Demonstrated modulation of a continuous light source has been shown at speeds above 10 GHz. Continued research should produce modulators at significantly higher frequencies.

The people in the materials research area are carrying out advanced structure development. Processing involving MBE and MOMBE (metallo-organic molecular beam epitaxy--a combination of MOCVD and MBE) is used to grow quantum well and superlattice structures. Their prime concern is to make sure they do not duplicate any research being done by the private sector. Once they can demonstrate a new structure and have control of the process, documentation is prepared and the technology is transferred to a commercial contract site or moved to a more "applied" activity within RSRE.

The device physics people use the material developed in the materials research area and actually build the quantum well and superlattice structures. These people are characterizing the properties of the structures to see if they are well defined and repeatable. The deposited layer materials have two-dimensional properties when the layers are relatively thin, rather than the three-dimensional properties of a non-layered substrate. Structures and devices involving more than 18 separate, deposited layers are being used in the research.

In the CAD area, the work centers on modeling the active devices that are being used in circuit development. The CAD people have found SPICE (a circuit design simulator developed originally at the University of California, Berkeley)

too restrictive to describe the devices and are using a new software package called ASTEC 3 for modeling and simulation. ASTEC 3 allows full mathematical description of the parameters of an active device, rather than forcing a fit to an existing mathematical model with adjustable parameters. A significant increase in model control is seen with this approach.

In the area of device fabrication, a relatively small but widely capable laboratory is used. The lab personnel routinely fabricate 2-inch wafers with both 0.5- and 0.25-micron gate-length E-beam DWW processes. The overall volume of the lab is relatively small, but extremely varied in capability.

5 STL

In STL's integrated circuits activity, both a GaAs R&D Division and a GaAs Pilot Fabrication Line exist. The pilot line has two processes, both of which are enhancement/depletion (E/D) processes. STL was the only company I saw in the UK that was involved in development of digital GaAs IC's. STL also has an analog and microwave capability and has demonstrated switched capacitor filters, transversal filters, and millimeter-wave (30 to 90 GHz) front ends.

The first process, which will also be the one used for the commercial offering, is a seven-mask, non-self-aligned, 1-micron gate-length E/D MESFET process with two layers of metalization. A sheet ion implant is used in the process as well as a chemical etch to recess the enhancement mode field effect transistor (EFET). The depletion mode field effect transistor (DFET) is typically not recessed. The second and more advanced process is a self-aligned implantation for n+ layer technology similar to what has been reported by Nippon Telegraph and Telephone Company (NTT) in Japan. 1.0- and 0.5-micron gate-length MESFET's are fabricated using a selective ion implantation process. Both processes use E-beam-generated contact masks; an E-beam DWW capability also exists. All processing is being done on 2-inch material at this time, but the capability exists for 3-inch material when required.

STL's commercial process will use the first process, and will offer standard E/D digital circuits such as prescalers and counters. STL has also demonstrated a small static random access memory (SRAM) capability (128 bits) for a specific application. Work is going on to develop an analog-to-digital converter, and they expect 4-bit accuracy at 1 GHz with an extension to 6 bits planned.

They feel that they have identified the source of the frequency-dependent drain conductance of the MESFET and are in the process of working on a fix for this significant problem. STL feels that their first process is capable of fabricating digital circuits up to a maximum of 3000 equivalent gates with operation at a quoted maximum speed of 500 MHz. No mention was made as to whether any gate arrays or standard cell offerings were going to be made. Their E/D process is reported to be very insensitive to temperature variation and will run on power supplies as low as 0.75 to 1.0 V and as high as 9.0 V. No electrostatic-induced damage (ESD) protection is incorporated, as they have not seen a large sensitivity to ESD.

On the analog side, the transversal filter is in production, operating in a range of 0 to 800 MHz with an output in the range of 0 to 3 MHz. The switched capacitor filter operates at a 250-MHz clock rate with a 10-MHz center frequency. Work is also being done on a high-gain amplifier such as might be used in an operational amplifier. It was while developing the high-gain amplifier that the frequency-dependent drain conductance proved to be a tough problem and inspired the research into the source of the problem.

As STC/STL (Standard Telephones and Cables/Standard Telecommunication Laboratories) has been dealing with commercial IC components for about 17 years, they have a complete design and test center capable of using commercially available IC foundry or standard cell offerings. Work stations for schematic

capture, simulation, and mask-level layout are part of the center. The significance of this center is that its expertise can be quickly put to use in developing STC's GaAs line of IC products. The people in the center are certainly product oriented and are knowledgeable in all aspects of IC utilization.

6 THOMSON-CSF

Thomson-CSF started GaAs research in the early 1970's. By 1975 they had already demonstrated an IC capability and by 1982 had a MESFET E/D process for digital applications. They currently have 4000 sq ft of clean room for GaAs processing and are building an additional 6000 sq ft for a production and manufacturing process line. The original 4000 sq ft will be used for process development when the new production fabrication facility is on line. They have their own material processing facility for producing normal Cr-doped liquid encapsulated Czochvalski (LEC) GaAs wafers and are bringing on line a low- pressure puller for low-defect indium-doped material. All material fabricated is 2 inch.

Thomson-CSF has plans to offer a variety of GaAs commercial products, and all of its identified digital products are based on depletion mode MESFET's using a buffered FET logic (BFL) topology. They plan to offer digital standard components, MMIC standard components, and custom foundry services capable of supporting both MMIC and digital circuits. Their standard process uses a 1.0-micron gate-length DFET with four pinch-off voltages available: -0.85 V for the gate array and standard cell designs, -1.2 or -1.3 V for the dividers, and -1.5 or -4.0 V for MMIC applications. Two metalization layers are used with a nitride isolation.

There are four divisions in the GaAs Department: Materials, Discrete Devices, Processing (30 people), and Products (46 people). I saw most of the Products Division; it consists of five sections: Digital Design (six people), MMIC Design (20 people), Linear Design (12 people), Test (five people), and CAD (three people).

Thomson-CSF has recently developed a 336-cell BFL gate array which will support about 1000 equivalent logic gates. Average power per cell is about 9 mW and toggle rates of 1.5 GHz have been measured over several thousand flip-flops. The array is designed for 80 percent utilization to keep the power dissipation to about 2.4 W. Internal gate delays are 125 ps to 155 ps (FI/FO=2) for temperatures between -55 and 125°C. The array also supports 38 emitter coupled logic (ECL)-compatible input/output (I/O) cells. Maximum yield seen for 60 cells is about 30 percent, for 180 cells is about 21 percent, and for 336 cells is about 11 percent.

In addition to the gate array, Thomson-CSF has developed a BFL standard cell offering that can support designs as large as 300 BFL gates or about 1000 equivalent logic gates. Internal gate delays are 120 ps at 5 mW/gate with a FO/FI=2. Maximum power dissipation should be less than 2 W, and ECL-compatible I/O cells exist for integration into a larger system. Average toggle rates of 1.1 GHz have been measured over several thousand 4-bit universal shift registers.

Their high-speed divider development group has designed both static and dynamic dividers. The static dividers use a single, clocked, latch topology while the dynamic dividers use a complementary clocked circuit. The complementary clock signals prove hard to generate and control, considering clock skew and asymmetrical loading problems. The dynamic dividers also show a much greater yield loss due to process variations than do the static designs. Designs demonstrated to date are shown in Table 1.

These dividers use the same type of ECL I/O cell as does the Gate Array. It should be noted that the ECL output I/O cell is designed to drive a 75-ohm load to -2.5 V.

7 PHILLIPS (LEP)

About 40 people are in LEP's GaAs Discrete Devices and IC's Division. They

Table 1

Divider Designs

#Gates	Function	Type (percent)	Max yield	Power	Frequency range
12	Div 2	Static	80-90	350 mW	30 MHz - 3.9 GHz
7	Div 2	Dynamic	80-90	350 mW	200 MHz - 3.9 GHz
24	Div 2/4	Dynamic	75	650 mW	200 MHz - 3.0 GHz
30	Div 4/5	Dynamic	25	750 mW	900 MHz - 3.0 GHz

are divided into five areas of work: digital processing, analog processing, digital design, analog design, and test and measurement. LEP has created a manufacturing division for their GaAs IC's to support both internal and external requirements. This manufacturing division, RTC, has at present about 50 people. As designs reach prototype and are completed, they are transferred to RTC for possible production for either an internal or external customer.

LEP's GaAs effort has several unique features. LEP grows its own material and makes its own wafers, as do several other companies. The big difference, according to LEP, is that its material is truly either defect free or is fabricated with an even distribution of defects. This material has been specifically developed for their large-scale integration (LSI) processes. The other difference between LEP and the rest of the GaAs IC manufacturers is that LEP has completely abandoned the depletion mode FET in its logic circuit design. All of its digital circuits strictly use normally off FET's or EFET's. LEP people feel that many of the parasitic problems associated with DFET's do not exist to the same extent in EFET's.

Research by LEP investigators has shown a definite correlation between variation in pinch-off voltage and the distribution of defects in the material. They have developed a high-density test FET pattern that has allowed them to characterize the pinch-off voltage (Vp) variation as a function of defect density and location on the wafer. They feel that control of Vp variations will enable higher speed operation at larger integration levels. They can also use this control to create voltage comparators that exhibit low-offset voltages which will allow improved analog-to-digital converter design on GaAs.

LEP's fabrication facility consists of 350 sq ft of clean room. They are now capable of producing 3000 wafers a year. Their standard process uses the 2-inch wafers produced by their low-pressure indium-doped system. A 1.0- or 0.7-micron gate length is standard with a self-aligned process available for 0.5-micron gates. The process uses a blanket silicon ion implantation and boron isolation coupled with a recessed gate technology. Two-layer metalization is available with a silicon nitride isolation. Typically, 6 to 10 masks are used, and these are E-beam-generated contact masks. The EFET pinch-off voltage for the LSI digital process is +150 mV.

LEP has demonstrated a 4×4 multiplier in a 2's complement format utilizing a pass transistor topology. Typical multiply time is 2 ns. They have developed a source-coupled FET logic (SCFL) gate array for one of their customers which operates at 5 mW per gate. The size is relatively small but it has difficult FI/FO requirements and must operate very fast. The same customer is also requiring a 1-K SRAM which must have an access time of 1.5 to 2.0 ns. This is presently being developed. A to D converter design is underway using the low-offset voltage comparators mentioned earlier. LEP people feel capable of achieving 4- to 6-bit accuracy now and expect to extend this to 8 bits.

They currently have a commercially available 100 MHz to 4.2 GHz asynchronous divide by 8. It uses their EFET-modified direct-coupled FET logic (DCFL) topology and requires a power supply of 1.5 to 2.0 V. Maximum frequency of operation is achieved with 4 to 6 dBm input at 50 ohms. Output is a 400 mV swing into a 50-ohm load. The die is 1 mm^2, and yield has been from 50 percent to 70 percent. In analog capability, LEP has demonstrated a variety of IC's. They started with a long history of discrete power FET's and have extended their capability to MMIC's as well. They have a 2- to 18-GHz amplifier with a gain of 5 dB based on a 0.5-micron gate HEMT design. The amplifier has a 1.2 dB noise figure at 12 GHz with 11 dB of associated gain. The HEMT is fabricated on MOCVD material that has been passivated with nitride. For internal use they are developing TV tuners in the UHF range as well as a 12-GHz direct broadcast satellite (DBS) receiver that includes GaAs mixers and VCO's. The VCO design is a wide-band design with a variable frequency of 1 octave. A variety of other analog designs exist, including power amplifiers in X-Band, phase amplifiers/splitters, 2- to 6-GHz high-gain amplifiers, and a wide variety of discrete devices.

8 SUMMARY

There is a wide range of effort in GaAs in both France and the UK. The approaches and the end goals are varied. Some of the companies will be able to provide advanced high-speed GaAs IC's, which will enable a significant improvement in the current military system technology. The other firms are too closely tied to R&D at the present time to provide a good manufacturing technology in the near future.

RSRE is excepted here, as it is a pure R&D laboratory. It is of key importance that GaAs IC manufacturing become a reality to provide the advanced components that the next generation of operational systems will be based upon. The transition from R&D to manufacturing is a tough one, but it is ultimately the test of the R&D that created the technology.

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